CLAIMS

1. An apparatus for computing floating-point operations wherein the apparatus receives an aligned addend comprising a plurality of bits and receives a plurality of products, comprising:

a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend;

a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and the products;

a compound adder that receives the output of the compression counter;

a carry network, wherein the carry network simultaneously computes an end-around-carry with at least some other computational operations and wherein the carry network receives the products and receives the output of the compression counter;

a selector, wherein the selector at least receives the output of at least some of the plurality of bits of the addend and wherein the selector al least receives the output of the carry network; and

a plurality of multiplexers (muxes), wherein the plurality of muxes receive outputs from the compound incrementer, the compound adder, and the selector.

2. The apparatus of Claim 1, wherein the compound incrementer further comprises:

an incrementer; and

a plurality of negation devices

3. The apparatus of Claim 2, further comprising the output of the incrementer inputs into at least one negation device of the plurality of negation devices.

4. The apparatus of Claim 3, wherein the plurality of negation devices are XOR-gates.

5. The apparatus of Claim 2, wherein the plurality of negation devices are XOR-gates.

6. The apparatus of Claim 1, wherein the carry network further comprises:

an XOR-gate; and

a carry generator.

7. The apparatus of Claim 4, wherein the carry network further comprises:

an XOR-gate; and

a carry generator.

8. The apparatus of Claim 1, wherein the carry network and the selector are at least configured to utilize a portion of the aligned addend to precompute a plurality of sets of select signals.

9. The apparatus of Claim 8, wherein the carry network further comprises at least the ability to compute a carry signal that is at least configured to select one set of select signals from the plurality of select signals.

10. The apparatus of Claim 1, wherein one mux of a plurality of muxes is at least configured to receive a sum signal from the compound adder, an incremented sum signal from the compound

adder, and an inverted sum of the compound adder producing at least a portion of an adder result.

11. The apparatus of claim 1, wherein the plurality of muxes is at least combined with a first stage mux of a normalizer into at least one multi-port mux.

12. The apparatus of claim 10, wherein the plurality of muxes is at least combined with a first stage mux of a normalizer into at least one multi-port mux.

13. The apparatus of Claim 1, wherein the compression device further comprises a 3:2 Counter.

14. The apparatus of Claim 4, wherein the compression device further comprises a 3:2 Counter.

15. The apparatus of Claim 7, wherein the compression device further comprises a 3:2 Counter.

16. A computer program product for computing floating-point

operations, wherein the computer program product receives an aligned addend comprising a plurality of bits and receives a plurality of products, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

a computer program product operating as a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend;

a computer program product operating as a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and the products;

a computer program product operating as a compound adder that receives the output of the compression counter;

a computer program product operating as a carry network, wherein the carry network simultaneously computes an end-around-carry with at least some other computational operations and wherein the carry network receives the products and received the output of the compression counter;

a computer program product operating as a selector, wherein the selector al least receives the output of at least some of the plurality of bits of the addend and wherein the selector al

least receives the output of the carry network; and

a plurality of computer program products operating as a plurality of muxes, wherein the plurality of muxes receive outputs from the computer program products operating as the compound incrementer, the compound adder, and the selector.

17. The computer program product of Claim 16, wherein the computer program product operating as compound incrementer further comprises:

a computer program product operating as an incrementer; and

a plurality of computer program products operating as negation devices.

18. The computer program product of Claim 17, further comprising the output of the computer program product operating as incrementer inputs into at least one computer program product operating as negation device of the plurality of a computer program products operating as negation devices.

19. The computer program product of Claim 18, wherein the plurality of computer program products operating as negation

devices are computer program products operating as XOR-gates.

20. The computer program product of Claim 17, wherein the plurality of computer program products operating as negation devices are computer program products operating as XOR-gates.

21. The computer program product of Claim 16, wherein the computer program product operating as carry network further comprises:

a computer program product operating as an XOR-gate; and

a computer program product operating as a carry generator.

22. The computer program product of Claim 19, wherein the computer program product operating as carry network further comprises:

a computer program product operating as an XOR-gate; and

a computer program product operating as a carry generator.

23. The computer program product of Claim 21, wherein the computer program products operating as the carry network and the selector are at least configured to utilize a portion of the

aligned addend to precompute a plurality of sets of select signals.

24. The computer program product of Claim 20, wherein computer program products operating as the carry network further comprises at least the ability to compute a carry signal that is at least configured to select one set of select signals from the plurality of select signals.

25. The computer program product of Claim 16, wherein one computer program product operating as mux of a plurality of computer program products operating as muxes is at least configured to receive a sum signal from the computer program products operating as the compound adder, an incremented sum signal from the computer program products operating as the compound adder, and an inverted sum of the computer program products operating as the compound adder producing at least a portion of an adder result.

26. The apparatus of claim 16, wherein the plurality of computer program products operating as muxes is at least

combined with a computer program products operating as first stage mux of a normalizer into at least one computer program products operating as multi-port mux.

27. The apparatus of claim 25, wherein the plurality of computer program products operating as muxes is at least combined with a computer program products operating as first stage mux of a normalizer into at least one computer program products operating as multi-port mux.

28. The computer program product of Claim 16, wherein the computer program product operating as compression device further comprises a computer program product operating as 3:2 Counter.

29. The computer program product of Claim 19, wherein the computer program product operating as compression device further comprises a computer program product operating as 3:2 Counter.

30. The computer program product of Claim 22, wherein the computer program product operating as compression device further comprises a computer program product operating as 3:2 Counter.